Paper No. 22

# A TRANSISTORISED AMPLIFIER FOR SEISMIC SIGNALS

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## SYNOPSIS

A transistorised directly coupled amplifier for the amplification of weak seismic signals is described. A low value of drift in the amplifier is obtained by using the two matched transistors in a differential configuration.

## INTRODUCTION

To improve the recording of very weak earthquakes, or micro-seisms, an electronic amplifier is used between the seismometer and the recorder as shown in Fig. 1. As the frequencies to be amplified are very low, of the order of 0-25 c/s, a directly coupled amplifier is used. The d. c. stability of the amplifier is affected by the poor regulation of power supplies and changes in ambient temperature. To obtain high d. c. stability, the differential configuration is employed with matched transistors and circuit elements.

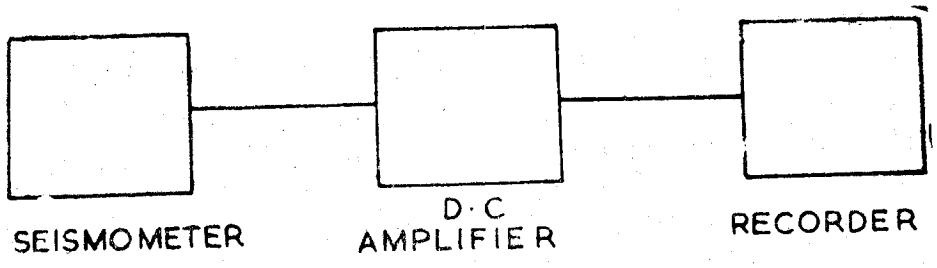


Fig. 1

To understand how differential amplifier provides a high d. c. stability, the general circuit of a differential amplifier as shown in Fig. 2 will be discussed first. In Fig. 2, neither of the input and the output terminals, is grounded, so the amplifier has floating input and output.

Let us assume that the amplifier of Fig. 2 is symmetrical and balanced i.e. $R_{1a}=R_{1b}$, $R_{2a}=R_{2b}$ and $\beta a=\beta b$ where $\beta$ is the common emitter current gain.

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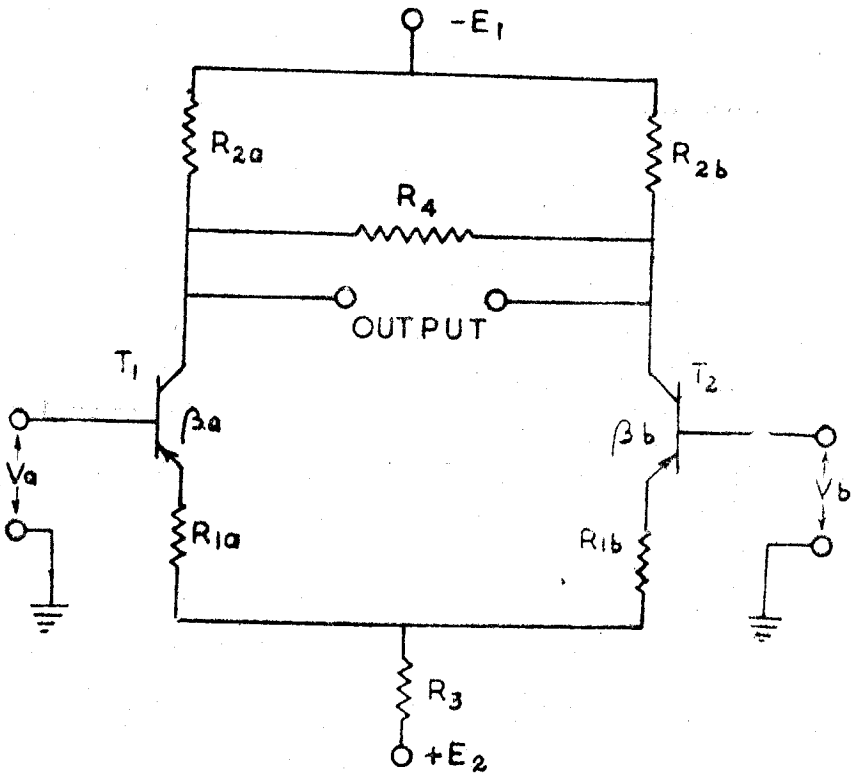


Fig. 2

If the two inputs 'Va' and 'Vb' are equal in magnitude and phase, then they are called 'inphase inputs' or 'common mode input signals'. As the circuit is balanced, the collector currents and collector voltages are same, and thus $R_4$ is connected between two homologous points. No current flows in $R_4$ and current in common element $R_3$ is twice that present in one side. Thus in a balanced circuit, common mode inputs do not produce any output. When 'Va' and 'Vb' are not equal in magnitude they can be replaced by their common mode equivalent input signal $Vc = \frac{Va+Vb}{2}$. If Va=Vb then Vc = Va = Vb. The common mode input signal is defined as the average of the signal voltages of the two input terminals with respect to ground.

If the two inputs 'Va' and 'Vb' are equal in magnitude, but opposite in phase, i.e. Va = — Vb, then they are called 'antiphase input' or 'differential mode input signals'. As the circuit is balanced, the collector currents of the two transistors, rise and fall equally, hence, the collector voltages of the two transistors are not equal. It means, $R_4$ is not connected between two equipotential points, and a virtual ground exists at the centre of $R_4$. The change in current flowing in $R_3$, due to two transistors, is equal and opposite, so no current flows in $R_3$ due to the input signals. Hence, in a balanced circuit the differential mode input signals produce differential output. When 'Va' and 'Vb' are not equal in magnitude, then they

can be replaced by their differential mode equivalent input signal. $Vd = \frac{Va-Vb}{2}$. If $Va = -Vb$, then $Vd = Va = -Vb$. The differential mode input signal is defined as half the difference of the signal voltages of the two input terminals with respect to ground.

Thus, CM signal is prevented from producing any output, by the negative feedback voltage developed across $R_3$. For DM signal, no current flows in $R_3$ and the emitters of two transistors are at virtual ground. The inherent discrimination of the circuit of Fig. 2 against common mode, in favour of differential mode input signals, leads to the name of 'differential amplifier'.

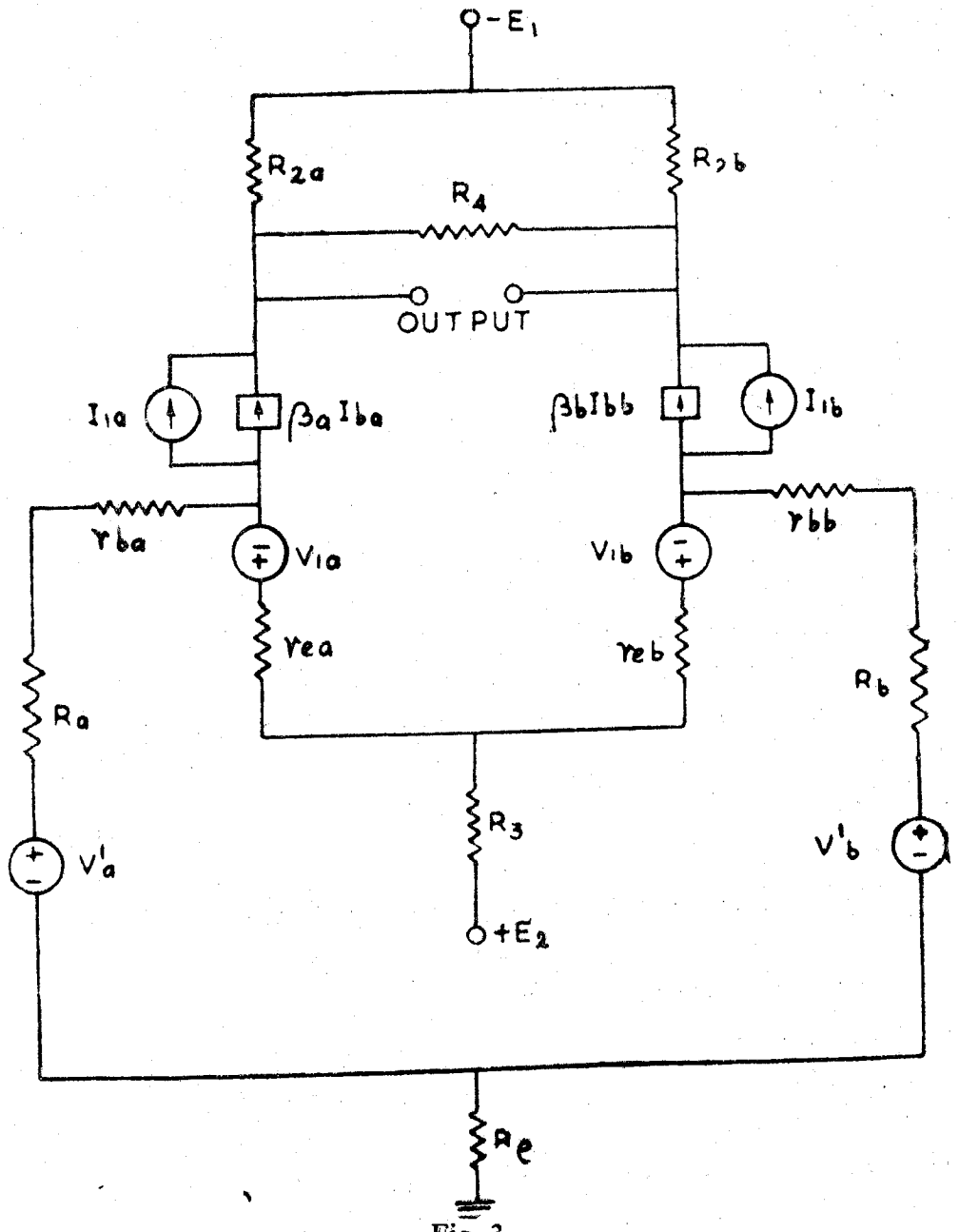


Fig. 3

**Effects of Circuit Unbalances**

In Fig. 3, the transistors are replaced by their common emitter T equivalent circuits. $V_{1a}$ and $V_{1b}$ are the forward biased base-emitter junction voltage drops, $I_{1a}$ and $I_{1b}$ the open base reverse saturation currents, $r_{ea}$ and $r_{eb}$ the internal emitter resistances, and $r_{ba}$ and $r_{bb}$ are the internal base resistances of the two transistors $T_1$ and $T_2$.

Next we consider the effects of unbalances in the circuit of Fig. 2. Let us suppose that all the homologous points of the circuit are balanced but $R_{2a}$ is not equal to $R_{2b}$. Now, if a pure CM signal (i.e. Va=Vb=Vc) is applied to the two input terminals of the two sides, the currents at the collectors of $T_1$ and $T_2$ will be equal because $\beta a = \beta b$. But the voltage drops in $R_{2a}$ and $R_{2b}$ will not be equal producing unequal voltages at the collectors of $T_1$ and $T_2$. This will make a differential output to be present. Hence unbalance between $R_{2a}$ and $R_{2b}$ has given a cross-coupling effect, whereby a CM input signal has produced a DM output. By analogous argument, a DM input signal will produce a CM output.

Similar cross-coupling effects will be produced, if unbalances are present in (1) $R_{1a}$ and $R_{1b}$ (2) $\beta a$ and $\beta b$, (3) $V_{1a}$ and $V_{1b}$ and (4) $I_{1a}$ and $I_{1b}$.

The base-emitter voltage drops $V_{1a}$ and $I_{1b}$ can be split into their CM and DM equivalent voltages $V_{1c}$ and $V_{1d}$. Similarly reverse saturation current $I_{1a}$ and $I_{1b}$ can be replaced by their CM and DM components.

Hence $V_{1c} = \frac{V_{1a}+V_{1b}}{2}$ $\qquad V_{1d} = \frac{V_{1a}-V_{1b}}{2}$

$V_{1c} = \frac{I_{1a}+I_{1b}}{2}$ $\qquad V_{1d} = \frac{I_{1a}-I_{1b}}{2}$

The CM output of the amplifier is produced by the following sources (1) CM input signal in the presence of emitter degeration due to $R_3$ (2) The two external CM supplies $E_1$ and $E_2$ (3) Internal generators $V_{1c}$ and $I_{1d}$ (4) DM input signal Vd (5) Internal DM generators $V_{1d}$ and $I_{1d}$.

Sources (4) and (5) will produce CM output only in the presence of circuit unbalances due to cross-coupling effects.

The DM output of the amplifier is produced by the following sources (1) External DM input signal Vd (2) The internal DM sources $V_{1d}$ and $I_{1d}$ (3) CM sources $V_c$, $E_1$, $E_2$, $V_{1c}$ and $I_{1c}$ in the presence of unbalances in the circuit.

**Expressions for the Different Parameters (Middle brook)**

As we are interested in DM output due to external DM input signal, and complete suppression of the CM input signals, the important parameters for this purpose are those for which the expressions are given below by equations (1) to (7) :

$$\text{CM voltage gain } A_{cc}=\frac{\alpha \cdot R_2}{R_1+2R_3} \tag{1}$$

$$\text{DM voltage gain } A_{dd}=\frac{\alpha}{R_1} \cdot \frac{R_2}{1+2R_2/R_4} \tag{2}$$

Common mode rejection factor (CMR) Hc is given by

$$\frac{1}{Hc}=\frac{R_1}{R_1+2R_3}\left(\frac{\delta R_2}{R_2}-\frac{\delta R_1}{R_1}+\frac{1}{1+\beta}\cdot\frac{\delta\beta}{\beta}\right) \tag{3}$$

CMR is defined as the ratio of CM input voltage to the DM input voltage to give same output voltage. It is a measure of how best a CM input is prevented from producing a DM output. In a balanced circuit value of Hc is infinity.

CM input admittance of the amplifier

$$Y_{cc}=\frac{1}{(\beta+1)(R_1+2R_3)} \tag{4}$$

DM input admittance of the amplifier

$$Y_{dd}=\frac{1}{(\beta+1)\cdot R_1} \tag{5}$$

CM to DM transfer input admittance

$$Y_{dc}=-\frac{1}{(1+\beta)(R_1+2R_3)}\cdot\left(\frac{\delta R_1}{R_1}+\alpha\cdot\frac{\delta\beta}{\beta}\right) \tag{6}$$

DM to CM transfer input admittance

$$Y_{cd}=-\frac{1}{(1+\beta)\cdot R_1}\left(\frac{R_1}{R_1+2R_3}\cdot\frac{\delta R_1}{R_1}+\alpha\cdot\frac{\delta\beta}{\beta}\right) \tag{7}$$

In an unbalanced circuit $Y_{dc}$ will be present producing DM output due to CM input. Similarly, $Y_{cd}$ produces CM output due to DM input. In a balanced circuit both will be zero.

In the above equations (1) to (7) the elements have following values:

$$R_1=\frac{R_{1a}+R_{1b}}{2}, \qquad \delta R_1=\frac{R_{1a}-R_{1b}}{2}$$

$$R_2=\frac{R_{2a}-R_{2b}}{2}, \qquad \delta R_2=\frac{R_{2a}-R_{2b}}{2}$$

$$\beta=\frac{\beta_a+\beta_b}{2}, \qquad \delta\beta=\frac{\beta_a-\beta_b}{2}$$

and $$\alpha=\frac{\beta}{\beta+1}$$

**Effects of Signal Source Impedance (Middle brook)**

In the derivation of the above equations, the impedance of the signal source was assumed to be zero. A differential amplifier whose two floating input terminals are at least partially isolated from ground, is necessarily driven from a three terminal signal source, even if the source impedance to ground is only stray coupling. A basic form of signal source with finite impedances is shown in Fig. 4, in which arbitrary source voltages '$V^1_a$' and '$V^1_b$' appear in series with source resistances 'Ra' and 'Rb'. Resistance Rc, common to both branches will be present, if no point of the source is grounded. The connection of the source with the input of the amplifier is shown in Fig. 3. Signal source resistances shown in Fig. 4 can be broken into its CM and DM components as follows:

$$\text{CM source impedance } Z^1_{cc} = R + 2R_c \tag{8}$$

$$\text{DM source impedance } Z^1_{dd} = R \tag{9}$$

$$\text{DM to CM source transfer impedance } Z^1_{cd} = \delta R \tag{10}$$

$$\text{CM to DM source transfer impedance } Z^1_{dc} = \delta R \tag{11}$$

where $$R = \frac{R_a + R_b}{2} \tag{12}$$

and $$\delta R = \frac{R_a - R_b}{2} \tag{13}$$

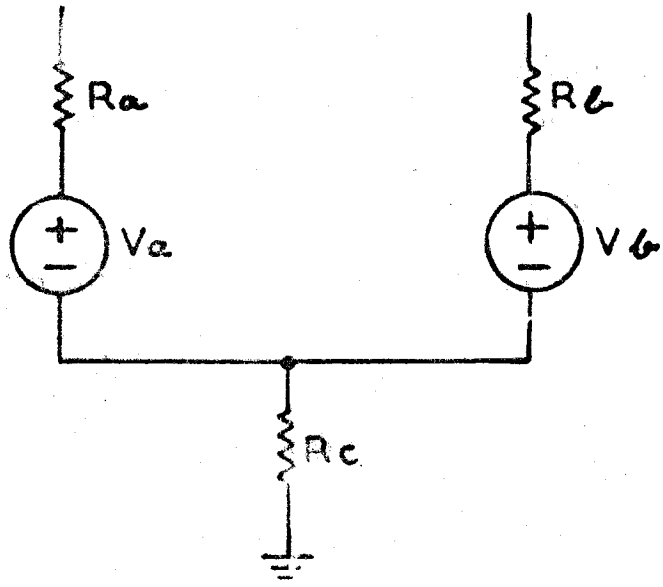


Fig. 4

By relating the amplifier input voltages to the source voltages, the following equations for the three important source parameters can be obtained:

$$(A_{dd})_s = \frac{1}{1 + Z^1_{dd} \cdot Y_{dd}} \tag{14}$$

$$(A_{cc})_s = \frac{1}{1+Z^1_{cc} \cdot Y_{cc}} \tag{15}$$

$$\left(\frac{1}{H_c}\right)_s = -\frac{Z^1_{dc} \cdot Y_{cc} + Z_{1dd} \cdot Y_{dc}}{1+Z^1_{cc} \cdot Y_{cc}} \tag{16}$$

In the equation (14), (15) and (16) subscript 's' corresponds to source. $Z^1_{dd}$, $Z^1_{cc}$ and $Z^1_{dc}$ are source impedances and $Y_{dd}$, $Y_{cc}$ and $Y_{dc}$ are the amplifier input admittance given by equations (4), (5) and (6).

Hence the total performance parameters of the amplifier and the signal source are:

$$(A_{cc})_t = (A_{cc})_s \cdot A_{cc} \tag{17}$$

$$(A_{dd})_t = (A_{dd})_s \cdot A_{dd} \tag{18}$$

$$\left(\frac{1}{H_c}\right)_t = \left(\frac{1}{H_c}\right)_s + \frac{(A_{cc})_s}{(A_{dd})_s \cdot H_c} \tag{19}$$

where subscript 't' stands for the total performance.

The adverse effects of the poor regulation of power supplies $E_1$ and $E_2$ on the d.c. stability of the amplifier can be reduced by having a high value of CMR.

Reducing the circuit unbalances or getting two transistors of nearly same $\beta$ is in our hand, but we have no control over the reverse saturation currents and base-emitter drops of two transistors. These two quantities are affected by ambient temperature changes, producing extraneous signals in the output. By selecting silicon transistors which have very low saturation currents, the effect of the saturation currents on the amplifier performance can be made very small. The two transistors $T_1$ and $T_2$ are strapped together in a clip so that variation in ambient temperature affects both the transistors in the same way, thus producing CM equivalent input signals at both the input basis. These signals can be prevented from producing any significant output by marking CMR very high.

The effect of CM equivalent input $V_{1c}$ corresponding to the base-emitter voltage drops of the two transistors can be reduced by having high CMR but the DM equivalent $V_{1d}$ will produce the undesirable DM output, which is not due to the input signals Va and Vb. Hence, the performance of the amplifier is limited by the mismatch of the base-emitter voltage drops of the two transistors $T_1$ and $T_2$.

The high value of CMR can be obtained by making $R_3$ as large as possible as seen from equation (3) but this will necessitate large value of $E_2$ to keep the same d.c. biasing conditions. The value of $E_2$ can be kept small if $R_3$ is replaced by a grounded base transistor whose high output impedance will act as $R_3$, without affecting the d.c. biasing conditions. For good performance $\beta$ of $T_1$ and $T_2$ should be as high as possible because it comes in the denominator of most of the equations of the parameters.

**Designed Circuit:**

The circuit shown in Fig. 5 was designed for collector currents of $T_1$ and $T_2$ each equal to half milli-amp., so the collector current of $T_3$ was slightly more than one milli-amp. The two transistors $T_1$ and $T_2$ were kept in contact with an aluminium clip, to keep the effects of ambient temperature changes on them as nearly equal as possible. Potentiometer P is used to get zero output for zero input at any one particular temperature generally room temperature. In the circuit following values of the components were used:

$T_1$, $T_2$ and $T_3$ = Mullard silicon transistors OC203

$E_1 = -12$ V, $E_2 = +9$ V

$R_{2a} = 15470$ ohms, $R_{2b} = 15500$ ohms

$$\delta R_2 = \frac{R_{2a} - R_{2b}}{2} = 15 \text{ ohms}$$

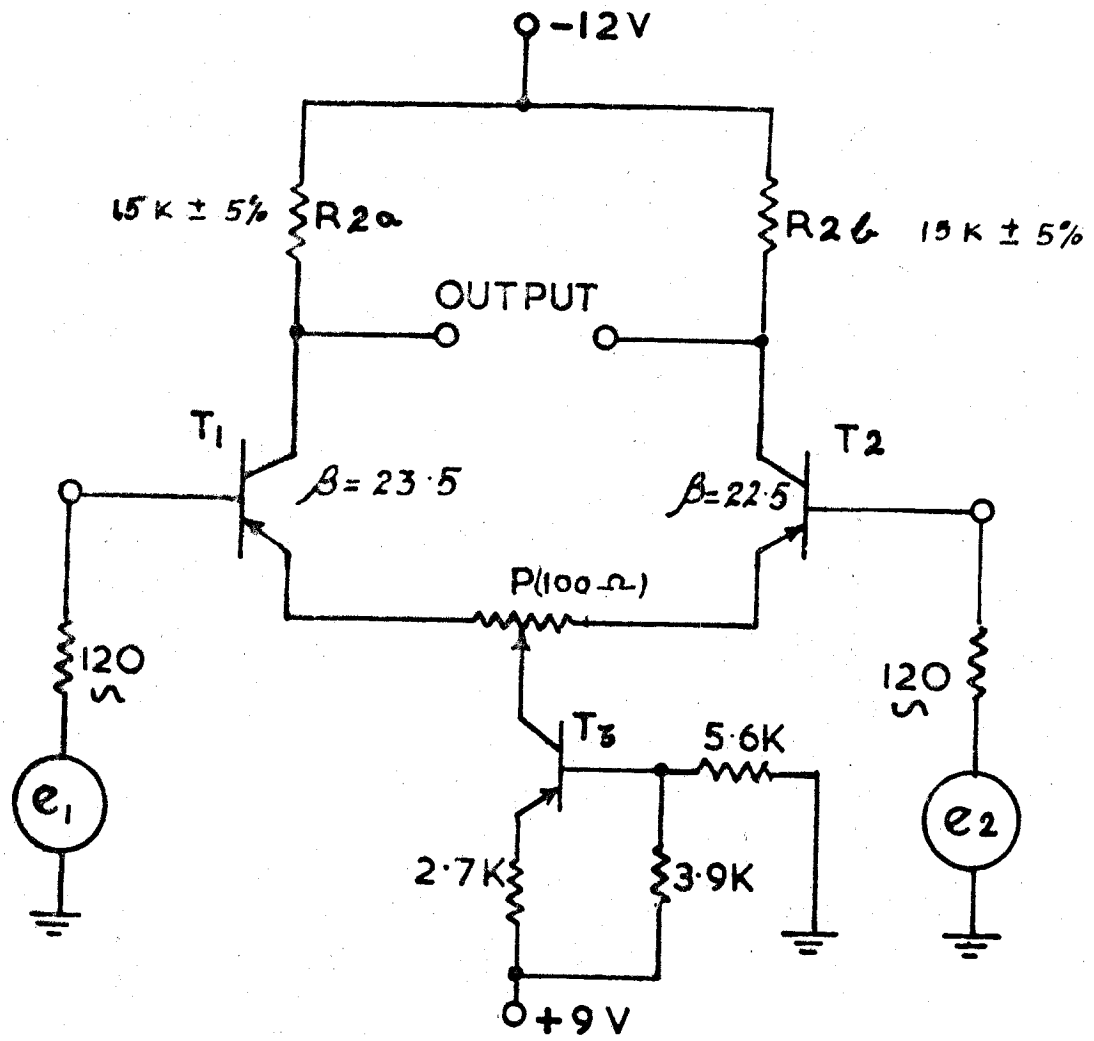


Fig. 5

$\beta_a = 23.5, \quad \beta_b = 22.5, \quad \delta\beta = \frac{\beta_a - \beta_b}{2} = 0.5$

$$\beta = \frac{\beta_a + \beta_b}{2} = 23$$

$V_{1a}=525$ mv, $V_{1b}=540$ mv

$V_{1c}=\frac{V_{1a}+V_{1b}}{2}=532.5$ mv, $V_{1d}=\frac{V_{1b}-V_{1a}}{2}=7.5$ mv

$P=100$ ohms potentiometer

$R_{1a}=R_{1b}=$Internal emitter resistance of $T_1$ or $T_2+P/2$

$=\frac{25}{\text{emitter current in mA}}+100/2$

$=100$ ohms.

To get zero output for zero input the setting of 'P' was 14 ohms away from the centre making $R_{1a}=50+64=114$ ohms and $R_{1b}+50+36=86$ ohms. Therefore

$$\delta R_1=\frac{114-86}{2}=14 \text{ ohms.}$$

The output resistance of $T_3$ at the operating point $Vce=-6v$ and $Ie=1.1$ mA was found to be nearly 70 K ohms.

The internal base-resistance $r_{ba}=r_{bb}$

$=20\times$(internal emitter resistance of transistor) approx.

$=20\times\frac{25}{.5\text{mA}}$

$=1000$ ohms.

In the experiment the impedance of each source of Fig. 5 was 120 ohms. The sources are in series with the internal base resistances of $T_1$ and $T_2$, one end of both the sources was grounded. For the source impedances we have

$R_a=R_b=1000+120=1120$ ohms

and $R_c=0$

From equation (8), (9), (12) and (13)

$R=\frac{R_a+R_b}{2}=1120$ ohms, $Z_{cc}=1120$ ohms

$Z_{dd}=R=1120$ ohms.

From equations (18) and (19), putting $R_4=$infinity

Overall DM voltage gain $(A_{dd})_t=100$ (20)

Overall CMR $(H_c)_t=4000$ (21)

From equations (2) and (3)

DM voltage gain of amplifier alone $A_{dd}=144$ (22)

CMR of amplifier alone HC=9,300 approx. (23)

The value of overall total DM gain ($A_{dd}$) t was in full agreement with the experimentally measured value. For higher DM gain the amplifier should have more than one stage.

**Frequency Response**

It was found to be flat from zero to 10 Kc/s and 3 db point was at 35 Kc/s. Frequency response curve is given in Fig. 6. Break in the curve is made in order to compress the curve in a similar space. Zero 'db' corresponds to a voltage gain of 100.

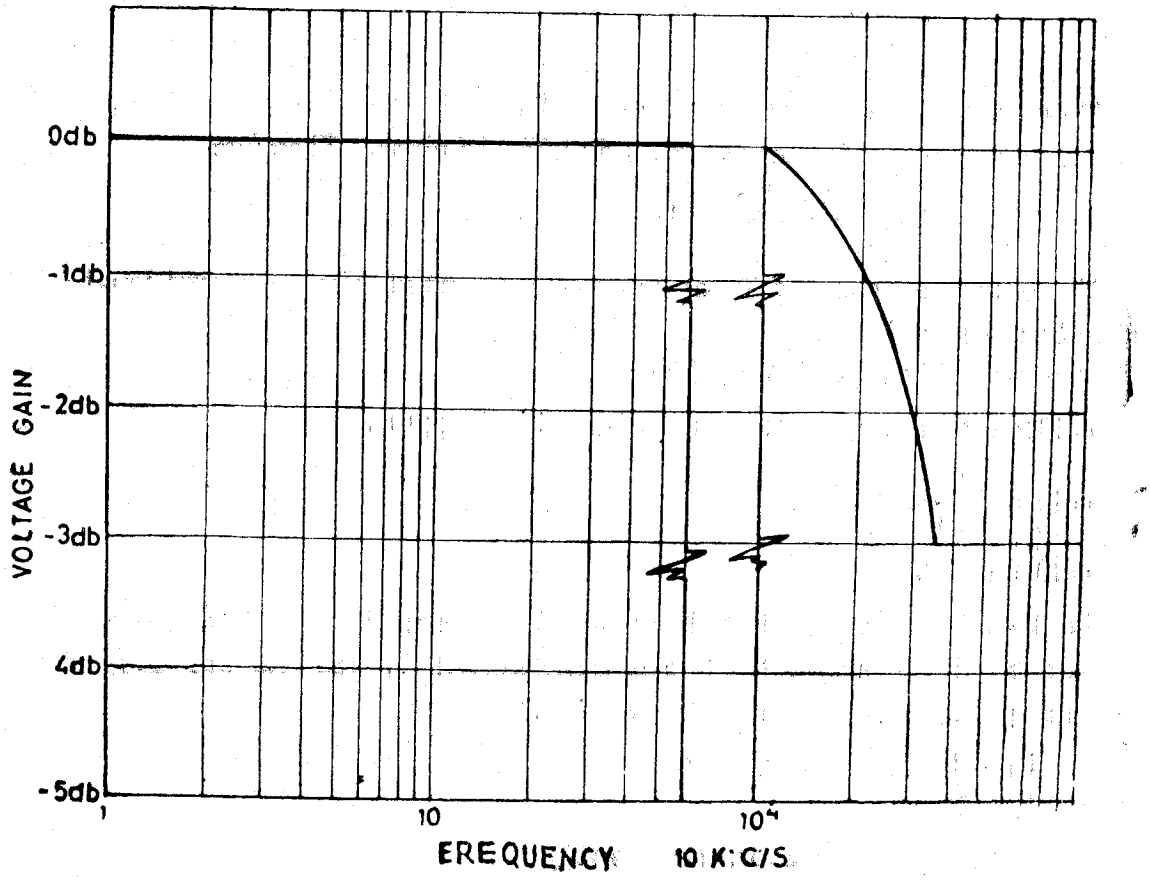


Fig 6

**Input and Output**

The amplifier can amplify a minimum signal of 2 mv. It can give a maximum output of 8 volts without distortion, thus giving a linear input-output characteristic up to the maximum output of 8 volts.

The base to collector reverse saturation current flows through the source resistance,

thus causing an undesired input signal. In silicon transistors, the reverse saturation current is very small, permitting use of a source having resistance up to few thonsands ohms, without producing any appreciable undesired input. Hence, the seismograph with high source resistance (e. g. Milne-Shaw Seismograph which has coil resistance of 1400 ohms), can be directly connected to the amplifier without the necessity of matching.

**Drift**

The drift was measured over a temperature range of 25°C to 75°C. Drift referred to input was found to be between 20 μv to 30 μv per degree centigrade rise of temperature.

## CONCLUSIONS

The performance parameters of the amplifier were found in the presence of the actual unbalances in the circuit. The author did not assume that the circuit is balanced. From equations (20) , (21) , (22) and (23) it is seen that if the source resistance is higher the DM voltage gain and value of CMR go down. Thus a seismograph producing a higher source resistance will degrade the performance of the amplifier more than that producing a lower source resistance.

## ACKNOWLEDGEMENT

The author is thankful to his colleagues, Mr. Hausila Singh and Mr. R. S. Mahajan for their valuable and kind suggestions from time to time during this work.

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